REMARKS

The present application has been amended in response to the Examiner's Office Action to place the application in condition for allowance. Applicant, by the amendments presented above, has made a concerted effort to present claims which clearly define over the prior art of record, and thus to place this case in condition for allowance.

In the Office Action, the Examiner objected to claims 14 and 27 for lacking antecedent basis. Claims 14 and 27 have been amended to overcome this objection, and therefore, it is respectfully requested that the Examiner's objection be withdrawn.

In the Office Action, the Examiner rejected the pending claims under 35 U.S.C. § 103(a) as being unpatentable over primarily United States Patent No. 6,218,848 (Hembrec et al.) and Japanese Publication No. 2002-148291 (Goto Nobumasa et al.). Applicant respectfully traverses.

Claim 1 specifically claims that the tester is configured to obtain a waveform from the DSO and store data in a file, and that the system includes means configured to use the data to calculate interconnect impedance versus time data for the DUT. Claim 15 is similar but is directed to a method (claiming that the DSO is configured to receive a reflected signal from the substrate and provide the reflected signal to the tester, that the tester is used to obtain a waveform and store data in a file, and that post processing software is used to analyze the data and provide interconnect impedance versus time data). Applicant respectfully submits that none of the cited references, including Hembree et al. (*848) and Goto Nobumasa et al. (*2002-148291), teach or suggest what is being claimed.

Hembree et al. ('848) does not even disclose a DSO, let alone that a tester receives a reflected signal from a DSO, that the data is stored in a file, and that the data is thereafter used to calculate interconnect impedance versus time data for the DUT. With regard to Figure 7, Hembree et al. merely describes (see col. 8, lines 46-67) measuring the resistance and using the measurement in a feedback system for generating test signals.

While Goto Nobumasa et al. (*2002-148291) discloses a TDR meter, and that the meter receives a reflected signal, Goto Nobumasa et al. does not disclose or suggest that the TDR meter provides the reflected signal to anything, such as a tester which is configured to obtain a waveform from the DSO and store data in a file, and that the data is thereafter used to calculate interconnect impedance versus time data for the DUT.

In view of the above amendments and remarks, Applicant respectfully submits that the claims of the application are allowable over the rejections of the Examiner. Should the present claims not be deemed adequate to effectively define the patentable subject matter, the Examiner is respectfully urged to call the undersigned attorney of record to discuss the claims in an effort to reach an agreement toward allowance of the present application.

Respectfully submitted,

Date: October 26, 2004

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Serial No. 10/620,057

Art Unit: 2829